

Programmer Pinouts

PICKit 2

1	VPP/ $\overline{\text{MCLR}}$
2	VDD Target
3	VSS (GND)
4	ICSPDAT/PGD
5	ICSPCLK/PGC
6	(Auxiliary)

MSP430 Spy Bi-Wire (14 pin header)

1	RESET (TDO/TDI)
2	VCC Tool
8	TEST
9	GND

AVR ISP-6

1	MISO
2	VCC
3	SCK
4	MOSI
5	$\overline{\text{RESET}}$
6	GND

AVR ISP-10

1	MOSI
2	VCC
3	(unused)
4	GND
5	$\overline{\text{RESET}}$
6	GND
7	SCK
8	GND
9	MISO
10	GND

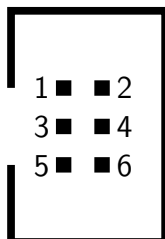
AVR JTAG

1	TCK
2	GND
3	TDO
4	VREF
5	TRS
6	nSRST
7	(unused)
8	nTRST
9	TDI
10	GND

BusPirate Mapping

BusPirate Name	ISP Name
MISO	MISO
3.3 V/5.0 V/(none)	VCC
CLK	SCK
MOSI	MOSI
CS	$\overline{\text{RESET}}$
GND	GND

Generic Boxed Header Pinout



As seen from top; numbering is equivalent to mapping via IDC connector to ribbon cable.

- PICKit 2 Programmer/Debugger User's Guide,
<http://ww1.microchip.com/downloads/en/DeviceDoc/51553E.pdf>
- AVR ISP Header Pinouts (Batsocks),
http://www.batsocks.co.uk/readme/isp_headers.htm
- AVR JTAG header pinout (JTAGtest),
<http://www.jtagtest.com/pinouts/avr>
- JTAG (MSP430),
[http://processors.wiki.ti.com/index.php/JTAG_\(MSP430\)](http://processors.wiki.ti.com/index.php/JTAG_(MSP430))

PIC 16F887

Key Electrical Specifications

2.0–5.5	V	Operating voltage range, at reduced clock speed
4.5–5.5	V	Operating voltage range, at full clock speed
± 25	mA	Maximum current per pin (absolute maximum rating)
± 95	mA	Maximum current in/out, total (absolute maximum rating)

External Components and Connections

2×	100 nF	ceramic cap	one per power input pin couple, widely considered best practice
2×	10 nF	ceramic cap	additionally if the ADC is used, one per power input pin couple

Pinout

re3/ $\overline{\text{mclr}}$ /vpp	□ 1	40	□ rb7/icspd
ra0/an0/ulpwu/c12in0-	□ 2	39	□ rb6/icspcl
ra1/an1/c12in1-	□ 3	38	□ rb5/an13/ $\overline{\text{t1g}}$
ra2/an2/vref-/cvref/c2in+	□ 4	37	□ rb4/an11
ra3/an3/vref+/c1in+	□ 5	36	□ rb3/an9/pgm/c12in2-
ra4/t0cki/c1out	□ 6	35	□ rb2/an8
ra5/an4/ $\overline{\text{ss}}$ /c2out	□ 7	34	□ rb1/an10/c12in3-
re0/an5	□ 8	33	□ rb0/an12/int
re1/an6	□ 9	32	□ vdd
re2/an7	□ 10	31	□ vss
vdd	□ 11	30	□ rd7/p1d
vss	□ 12	29	□ rd6/p1c
ra7/osc1/clkin	□ 13	28	□ rd5/p1b
ra6/osc2/clkout	□ 14	27	□ rd4
rc0/t1oso/t1cki	□ 15	26	□ rc7/rx/dt
rc1/t1osi/ccp2	□ 16	25	□ rc6/tx/ck
rc2/p1a/ccp1	□ 17	24	□ rc5/sdo
rc3/sck/scl	□ 18	23	□ rc4/sdi/sda
rd0	□ 19	22	□ rd3
rd1	□ 20	21	□ rd2

- PIC16F882/883/884/886/887 Data Sheet
<http://ww1.microchip.com/downloads/en/DeviceDoc/40001291H.pdf>

ATmega 328P

Key Electrical Specifications

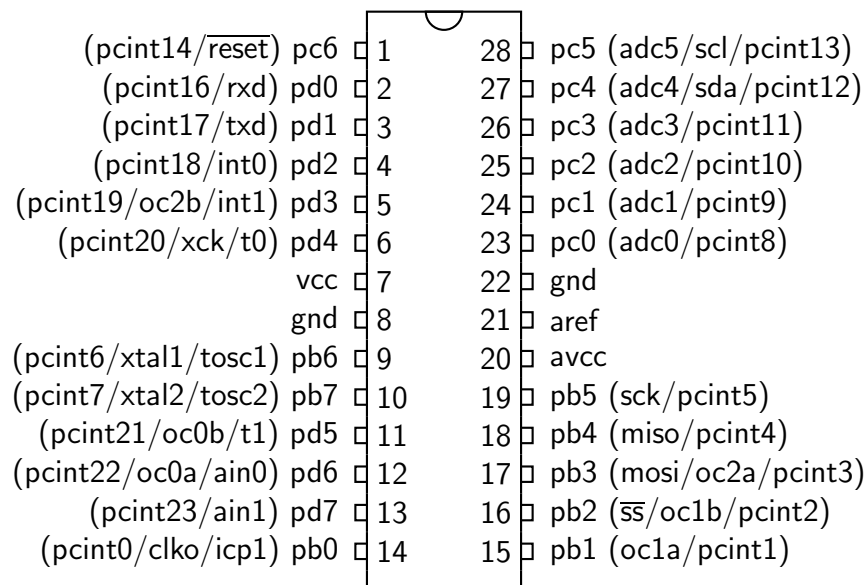
1.8–5.5	V	Operating voltage range, at reduced clock speed
4.5–5.5	V	Operating voltage range, at full clock speed
± 40	mA	Maximum current per pin (absolute maximum rating)
± 200	mA	Maximum current in/out, total (absolute maximum rating)

External Components and Connections

1×	10 kΩ	resistor	between RESET and VCC
1×	100 nF	ceramic cap	between VCC and GND
1×	100 nF	ceramic cap	between AREF and GND if ADC is used

- AVCC and VCC should be externally connected; if the ADC is actually used, use a low pass filter (see datasheet), otherwise connect directly.
- If the fuse bits are set accordingly, then an external clock source/oscillator/resonator may also be required to even program the device.

Pinout



- Datasheet Summary
http://www.atmel.com/Images/Atmel-42735-8-bit-AVR-Microcontroller-ATmega328-328P_Summary.pdf
- Datasheet Complete
http://www.atmel.com/Images/Atmel-42735-8-bit-AVR-Microcontroller-ATmega328-328P_datasheet.pdf

MSP430 G2553

Key Electrical Specifications

- 1.8–3.6 V Operating voltage range, at full clock speed
- ± ??? mA Maximum current per pin
- ± 48 mA Maximum current in/out, total

External Components and Connections

- 1× 47 kΩ resistor between RESET and VCC
- 1× 2.2 nF ceramic cap between RESET and GND
- 1× 100 nF ceramic cap between VCC and GND
- 1× 10 μF electrolytic cap between VCC and GND (only for ADC?)

Pinout

	dvcc	□ 1	20	□ dvss
	p1.0/ta0clk/aclk/a0/ca0	□ 2	19	□ xin/p2.6/ta0.1
	p1.1/ta0.0/uca0rx/uca0somi/a1/ca1	□ 3	18	□ xout/p2.7
	p1.2/ta0.1/uca0txd/uca0simo/a2/ca2	□ 4	17	□ test/sbwtck
	p1.3/adc10clk/caout/vref-/veref-/a3/ca3	□ 5	16	□ $\overline{\text{rst}}$ /nmi/sbwt dio
p1.4/sclk/ucb0ste/uca0clk/vref+/veref+/a4/ca4/tck		□ 6	15	□ p1.7/caout/ucb0simo/ucb0sda/a7/ca7/tdo/tdi
p1.5/ta0.0/ucb0clk/uca0ste/a5/ca5/tms		□ 7	14	□ p1.6/ta0.1/ucb0somi/ucb0scl/a6/ca6/tdi/tclk
	p2.0/ta1.0	□ 8	13	□ p2.5/ta1.2
	p2.1/ta1.1	□ 9	12	□ p2.4/ta1.2
	p2.2/ta1.1	□ 10	11	□ p2.3/ta1.0

- MSP430G2x53 MSP430G2x13 Mixed Signal Microcontroller Datasheet
<http://www.ti.com/lit/ds/symlink/msp430g2553.pdf>
- MSP430x2xx Family User's Guide
<http://www.ti.com/lit/ug/slau144j/slau144j.pdf>